**CS 5160-00 FPGA Architecture & CAD** Fall 2018

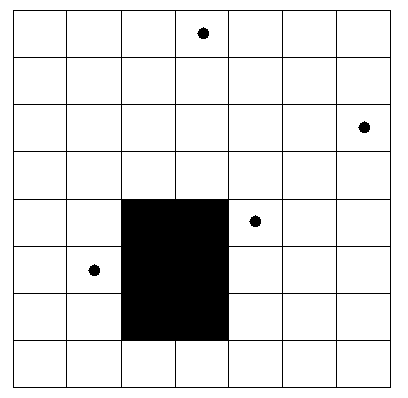
**Homework 4 (Due: Dec. 17, 2018)**

1. Consider the FPGA architecture shown on p.13 of Unit 12. Suppose the resource requirement of modules *p* and *q* are <14, 3, 1> and <6, 0, 2>, respectively.

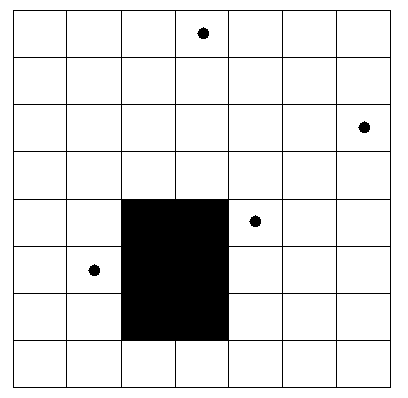
(i) Give the (width, height) of each element in the irreducible realization list *Lp*(0,0).

(ii) Suppose *u* is a slicing floorplan with module *p* on the left of module *q* as shown below. Compute the irreducible realization list *Lu*(0,0).

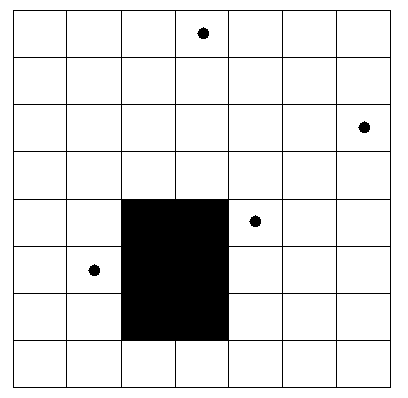
1. Describe in a few sentences what is meant by iterative negotiation-based routing as used by the VPR router.
2. VPR uses an incremental technique when routing a multi-terminal net with maze expansion. Apply it to route the following multi-terminal net assume we expand from the source *S* at the beginning. Clearly show your steps and use a different figure to show the work for each stage.



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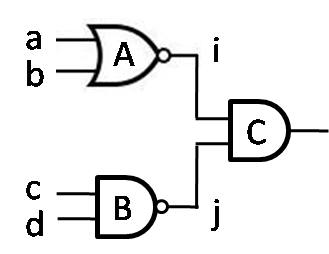


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1. Consider a circuit and a FPGA based on 2-LUTs like the one below.

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(a) Suppose we implement the circuit on the FPGA by mapping each of gates *A*, *B*, and *C* to one LUT. Show the contents and the connections of the three LUTs used.

(b) Assume the static probabilities of signals *a*, *b*, *c*, and *d* are independent and are equal to 0.6, 0.5, 0.5 and 0.3, respectively. What are the static probabilities of signals *i* and *j*?

(c) Assume that on average the leakage power of a MUX is smaller when its output is 1 than when its output is 0. For maximum leakage power reduction, should we invert only signal *i*, or only signal *j*, or both, or none of them? Show the new contents and the connections of the three LUTs after performing the desired inversion(s).

1. Consider a FPGA based on 3-LUTs and the same circuit in problem 4. Suppose gates A and C are mapped into one LUT while gate B is mapped into another LUT. Show a configuration of the LUTs (i.e., SRAM cell content and selection signal assignment) that minimizes unnecessary toggling within the LUTs for dynamic power optimization.